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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,039	06/20/2003	Oliver Chyan	122302.00001	6398

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Michael G. Cameron
Jackson Walker LLP
Suite 600
2435 North Central Expressway
Richardson, TX 75080

EXAMINER	
LE, DUNG ANH	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No.	Applicant(s)	
	10/600,039	CHYAN ET AL.	
	Examiner	Art Unit	
	DUNG A LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,25-29,31-34,47 and 48* is/are pending in the application.

4a) Of the above claim(s) *11-24,30 and 35-47* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,25-29,31-34 and 48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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DETAILED ACTION

In light of Amendment, the previous Office action is withdrawn. This is a new ground of rejection.

Claim Rejections

Set of claims 1- 10

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 8 and 10 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Huang et al. (6831003) in view of Choi (59637533).

Huang et al. teaches that a method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

preparing an inter-level dielectric substrate106;

depositing a layer of Ru 204 on the inter-level dielectric substrate;

depositing a additional layer 212(210) as a diffusion stuffer on the Ru layer; and

depositing copper 208 on the additional layer 212.

Huang does not teach depositing copper on a additional layer made off RuO2.

Choi teaches that depositing copper on RuO2 layer 10 as diffusion barrier (col 5, line 50, fig. 1F, col 1, lines 38-45, col 2, line 66).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the additional layer into RuO2 barrier Huang 's method, in order to obtain the best resultant copper diffusion barrier (also refer to column 7, line 8-30).

Regarding claim 8, depositing the RuO2 using a thermal oxidation technique (col. 2, lines 40-45).

Regarding claim 10, depositing the RuO2 using physical vapor deposition (col 1, line 13).

Claims 7 and 9 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Huang et al. (6831003) in view of Choi (59637533) and further in view of the following remark.

Huang in view of Choi discloses the claimed invention as applied to claim 1 including the step of depositing the RuO2 layer on the inter-level dielectric using a thermal oxidation technique (Choi, col 2, lines 40-45) and depositing the RuO2 layer on the inter-level dielectric using a physical vapor technique (Choi col 1, line 17) except for depositing the RuO2 layer on the inter-level dielectric using an atomic layer technique and depositing the RuO layer on the inter-level dielectric using an electrochemical technique.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to depositing the RuO2 layer on the inter-level dielectric using an atomic layer technique and depositing the RuO layer on the inter-level dielectric using an electrochemical technique to form RuO2, because the abovementioned methods are commonly used to prevent undesirable or detrimental reactions in the contact region, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the desired application.

Claims 2, 4 and 6 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Huang et al. (6831003) in view of Choi (59637533) and further in view of the following remark(s).

Regarding claim 2, Huang in view of Choi discloses the claimed invention as applied to claim1 except for depositing multiple layers of Ru and RuO2 between the inter-level dielectric substrate and the copper layer.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form multiple layers of Ru and RuO2 between the inter-level dielectric substrate and the copper layer, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art.

Regarding claim 4, depositing the RuO2 layer using a thermal oxidation technique (col 2, lines 40-45).

Regarding claim 6, depositing the RuO2 using physical vapor deposition (col 1, line 13).

Regarding claims 3 and 5, Huang in view of Choi discloses the claimed invention as applied to claims 1-2 including the step of depositing the RuO2 layer on the inter-level dielectric using a thermal oxidation technique (Choi, col 2, lines 40-45) and depositing the RuO2 layer on the inter-level dielectric using a physical vapor technique (Choi col 1, line 17) except for depositing the RuO2 layer on the inter-level dielectric using an atomic layer technique and depositing the RuO layer on the inter-level dielectric using an electrochemical technique.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to depositing the RuO2 layer on the inter-level dielectric using an atomic layer technique and depositing the RuO layer on the inter-level dielectric using an electrochemical technique to form RuO2, because the abovementioned methods are commonly used to prevent undesirable or detrimental reactions in the contact region, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use.

Set of claims 25- 29.

Claims 25, 28- 29 are rejected under 35 USC 102 (b) as being anticipated by Choi (5637533).

Choi teaches a method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising: preparing an inter-level dielectric substrate 5; depositing one or a plurality of layers 10 of RuO2 (by the step of depositing of Ru on the substrate followed by the implantation of oxygen into the Ru layer , also see MPEP 2111: ... it is not proper to read limitations appearing in the specification into the claim when the limitation not cited in the claim. See In re Paulsen,...) on the inter-level dielectric substrate; and depositing copper 11 on the RuO2 layer (figs.1E-1F and related texts).

Regarding claim 28, depositing the RuO2 layer on the inter-level dielectric using a thermal oxidation technique (Col 2, lines 40-50).

Regarding claim 29, depositing the RuO2 layer on the inter-level dielectric using a physical vapor technique (col 1, lines 15- 20).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 26- 27 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Choi (5637533) in view of the following remark.

Choi discloses the claimed invention as applied to claim 25 including the step of depositing the RuO2 layer on the inter-level dielectric using a thermal oxidation technique (col 2, lines 40-45) and depositing the RuO2 layer on the inter-level dielectric using a physical vapor technique (col 1, line 17) except for depositing the RuO2 layer on the inter-level dielectric using an atomic layer technique and depositing the RuO layer on the inter-level dielectric using an electrochemical technique.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to depositing the RuO2 layer on the inter-level dielectric using an atomic layer technique and depositing the RuO layer on the inter-level dielectric using an electrochemical technique to form RuO2, because the abovementioned methods are commonly used to prevent undesirable or detrimental reactions in the contact region, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use.

Set of claims 31- 32.

Claim 31 is rejected under 35 USC 102 (e) as being anticipated by Iwasaki et al. (2004/0238965 A1).

Iwasaki et al. teach a method of controlling copper diffusion during the integration of copper interconnects 10 during integrated circuit fabrication, comprising using Ru as a

diffusion barrier 9/11 in fig. 1 (see MPEP 2111: ... it is not proper to read limitations appearing in the specification into the claim when the limitation not cited in the claim. See In re Paulsen,...).

Claims 31-32 are rejected under 35 USC 102 (e) as being anticipated by Huang et al. (6831003 B1).

Huang et al. teach a method of controlling copper diffusion during the integration of copper interconnects 208 (figs. 6-10 and related textsespecially refer to column6,lines 30-47) during integrated circuit fabrication, comprising using Ru 204 as a diffusion barrier

Regarding claim 32, further comprising eliminating a copper seed layer (col 6,line 55).

Set of claims 33-34.

Claims 33-34 are rejected under 35 USC 102 (e) as being anticipated by Iwasaki et al. (6,624,513).

Iwasaki et al. teaches a method of controlling copper diffusion during the integration of copper interconnects during integrated circuit fabrication, comprising using Ru (col 12, lines 20-31) and RuO2 (col 12, lines 54-56) as a diffusion barrier.

Regarding claim 34, further comprising eliminating a copper seed layer (fig. 13).

Independent claim 47 (Newly submitted claim)

Newly submitted claim 47 directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: claim 47 having a step

of depositing a layer of RuO2 as a diffusion stuffer on the inter-level dielectric substrate; depositing a layer of Ru on the RuO2; and depositing copper on the Ru layer, wherein the method eliminates the need for a copper seed layer.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits.

Accordingly, claim 47 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Independent claim 48 (newly added claim)

Claim 48 is rejected under 35 USC 102 (e) as being anticipated by Iwasaki et al. (6,624,513).

Iwasaki et al. discloses a method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

preparing an inter-level dielectric substrate 21;

depositing one or a plurality of layer of RuO2 or Ru (22a, col 12, line 26) or a combination thereof on the inter-level dielectric substrate 21; and

depositing copper 23 on the RuO2 or Ru 22a or a combination thereof,

wherein the method eliminates the need for a copper seed layer (fig. 13).

Claim 48 is rejected under 35 USC 102 (b) as being anticipated by Choi (5637533).

Choi discloses a method of controlling and containing copper diffusion during the integration of copper interconnects during the fabrication of integrated circuits, comprising:

preparing an inter-level dielectric substrate;

depositing one or a plurality of layer of RuO2 10 (by the step of depositing of Ru on the substrate followed by the implantation of oxygen into the Ru layer , also see MPEP 2111: ... it is not proper to read limitations appearing in the specification into the claim when the limitation not cited in the claim. See In re Paulsen,...) or Ru or a combination thereof on the inter-level dielectric substrate; and

depositing copper 11 on the RuO2 10 or Ru or a combination thereof,

wherein the method eliminates the need for a copper seed layer (fig. 1F).

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The central fax phone numbers for the organization where this application or proceeding is assigned are (571)272-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE
Primary Examiner
Art Unit 2818